In the Claims:

Amend the claim set, without prejudice, as detailed in the following complete listing of all claims (1 to 15):

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)

8. (New) A light emitting semiconductor package including:

a) a semiconductor chip having a top surface and a bottom surface and including at least one light emitting device formed in the chip which can emit electromagnetic radiation, the at least one light emitting device residing on or in the top surface; and

b) a first hollow cap including:

(1) a central portion and first perimeter walls extending from the perimeter edge of the central portion with the free edges of the first perimeter walls bonded to the top surface to provide a first cavity;

(2) the central portion overlying at least part or all of the at least one light emitting device; and

(3) at least one region of the central portion which is substantially transparent or translucent to the electromagnetic radiation;

wherein the first hollow cap has been bonded to the semiconductor chip at the wafer stage prior to separation of the wafer into individual packages.

9. (Re-presented – formerly dependent claim 2) The package of claim 8 wherein the at least one region refracts said electromagnetic radiation emitted by said at least one device.

10. (Re-presented – formerly dependent claim 3) The package of claim 8 wherein the cap further includes at least one attachment means for attaching an electromagnetic radiation transmitting cable or fiber to the cap, whereby at least some electromagnetic radiation emitted from the at least one device passes through said at least one region into the cable or fiber.

11. (Re-presented – formerly dependent claim 4) The package of claim 10 wherein the at least one attachment means includes a second perimeter wall extending from the periphery of the central portion away from the first perimeter wall.

12. (Re-presented – formerly dependent claim 5) The package of claim 10 wherein the at least one attachment means includes at least one recess in the central portion.

13. (Re-presented – formerly dependent claim 6) The package of claim 8 further including a second cap bonded to the bottom surface of the chip.

14. (Re-presented – formerly dependent claim 7) The package of claim 8 further including a second cap bonded to the bottom surface of the chip, said second cap, in plan view, overlaying part or all of the at least one device.

15. (New) The package of claim 9 wherein more than one region of the central portion is provided, each region of the central portion associated with at least one light emitting device.

REMARKS

New claim 8 is a new version of cancelled claim 1. New claim 8 more clearly presents the essential elements of the invention. Basis for new claim 8 can be found from the disclosures at page 11, line 29 to page 12, line 29 with reference to Figure 28. For example, Figure 28 discloses a light emitting semiconductor package 250; including:

a) a semiconductor chip 252 having a top surface and a bottom surface and including at least one light emitting device 254 formed in the chip 252 which can emit electromagnetic radiation, the at least one light emitting device 254 residing on or in the top surface; and

b) a first hollow cap 256 including:

(1) a central portion 260 and first perimeter walls extending from the perimeter edge of the central portion 260 with the free edges of the first perimeter walls bonded to the top surface to provide a first cavity;

(2) the central portion 260 overlying at least part or all of the at least one light emitting device 254; and

(3) at least one region 258 of the central portion 260 which is substantially transparent or translucent to the electromagnetic radiation;

wherein the first hollow cap 256 has been bonded to the semiconductor chip 252 at the wafer stage prior to separation of the wafer into individual packages.

Re-presented claims 9 to 14 are formerly claims 2 to 7, now made dependent from new claim 8.

New claim 15 states that more than one region of the central portion is provided, each region of the central portion associated with at least one light emitting devices. Basis for this new claim is found in at least Figure 28, where more than one region 258 of the central portion 260 is provided, each region 258 of the central portion 260 associated with at least one light emitting device 254.

35 USC 102(b)

At page 2 of the Office Action, the Examiner rejects claims 1-5 under 35 USC 102(b), as being anticipated by Jewell *et al.* (US 5,500,540). A claim is anticipated if all of its limitations are present in a single reference in the prior art. Because all of the limitations of new claim 8 of the present invention are not present in Jewell *et al.*, as discussed below, new claim 8, and re-presented dependent claims 9-15, are not anticipated by Jewell *et al.* Reconsideration and withdrawal of the rejection is respectfully requested.

New claim 8 requires "a first hollow cap including a central portion and first perimeter walls extending from the perimeter edge of the central portion with the free edges of the first perimeter walls bonded to the top surface to provide a first cavity". It is respectfully submitted that no such feature is disclosed in Jewell *et al.*

In Jewell *et al* the optical chips 28 are integrated to the optoelectronic wafer 42 by material deposition, spin casting or physical mounting (col. 5, ln. 58). In the cases of deposition and spin casting an optical chip 28 cannot be formed as a hollow cap. The techniques described in Jewell *et al* allow only a solid optical chip to be constructed on the optoelectronic wafer 42. Furthermore, in the case of physically mounting an optical chip 28, Jewell *et al* only discloses and suggests use of a solid block of material, not a hollow cap as in claim 8 of the present application.

At col. 6, ln. 30-36 of Jewell *et al*: "Referring now to FIG. 3A, there is shown a means for integrating optical elements 30 to optoelectronic wafer 42 to form wafer package 53 by physically mounting optical wafer 54 onto optoelectronic wafer 42. Both optoelectronic wafer 42 and optical wafer 54 are typically a few hundred micrometers thick, however, either or both wafers could vary greatly in thickness". This demonstrates that the optical wafer 54 (i.e. optical chip 28) disclosed is of substantially uniform thickness.

Furthermore, at col. 6, ln. 57: "...it is also possible to use projections 70 on the bottom face 66 [of] optical wafer 54 which fit into holes 72 in optoelectronic wafer 42". This also demonstrates that the optical wafer 54 (i.e. optical chip 28) disclosed is not a "hollow cap including a central portion and first perimeter walls" (from new claim 8) as a hollow region cannot hold projections.

Still furthermore, at col. 7, ln. 27: "A major portion of the thickness of optoelectronic wafer 42 or of optical wafer 54 may be removed, thereby forcing the thinned wafer to expand or contract with the other wafer". This further demonstrates that the optical wafer 54 (i.e. optical chip 28) disclosed is not a "hollow cap including a central portion and first perimeter walls" (from new claim 8) as if a hollow cap was intended to be disclosed in Jewell *et al* then thinning the optical wafer would remove the perimeter walls. Clearly, it is intended that the optical wafer 54 is a solid block of material.

Yet furthermore, at col. 8, ln. 23: "Referring now to FIG. 5, there is shown generic optical chip 80...". To be described as generic the optical chip 80 must show characteristics relating to all optical chips in Jewell *et al*. In Figure 5, the optical chip 80 is clearly shown as a solid block without a hollow or perimeter walls. The optical chips disclosed in Jewell *et al* do not anticipate the feature of the hollow cap of the presently claimed invention.

It is respectfully submitted that the optical chip 28 shown in Figure 1 or Figure 2 does not disclose a "hollow cap...with the free edges of the perimeter walls bonded to the top surface to provide a first cavity". Nowhere in the specification of Jewell *et al* is it disclosed, suggested or taught that free edges of a hollow cap are bonded to the optoelectronic wafer 42.

The skilled person reading the specification in its entirety is clearly only taught that the optical chip 28 is a solid feature. The Examiner's interpretation of the optical chip 28 in Figure 1 or Figure 2 being hollow is respectfully submitted to be incorrect. Any such appearance is clearly a drawing artifact after having read the complete specification. It is submitted that the optical chip 28 in Figure 1 or Figure 2 is not shown to be hollow, rather a view is presented that more clearly shows the internal beams of light 16 in the optical chip 28. The interpretation that the optical chip 28 is shown as a hollow cap does not agree with the teachings of the specification for at least the reasons presented in the preceding paragraphs.

35 USC 103(a)

At page 3 of the Office Action, the Examiner rejects claims 6-7 (re-presented as claims 13-14) under 35 USC 103(a) as being unpatentable over Jewell *et al.* in view of Bloom (US

5,805,757). Obviousness can only be established by combining or modifying teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge generally available to one skilled in the art. Reconsideration and withdrawal of this objection is respectfully requested for the reasons presented below.

Jewell *et al* does not disclose a "a first hollow cap including a central portion and first perimeter walls extending from the perimeter edge of the central portion with the free edges of the first perimeter walls bonded to the top surface to provide a first cavity", for the reasons presented in the preceding section. Neither does anything in Bloom disclose or suggest such a feature. The combination of Jewell *et al* and Bloom does not teach the first hollow cap of new claim 8 of the present application. It is respectfully submitted that new claim 8 is patentable over Jewell *et al* in view of Bloom. As re-presented claims 13-14 depend from new claim 8, it is likewise submitted that claims 13-14 are patentable over Jewell *et al* in view of Bloom.

Moreover, re-presented claims 13-14 require a "second cap bonded to the bottom surface of the chip". It is respectfully submitted that Bloom does not disclose such a feature as the Examiner suggests. The Examiner relies on Figure 9A and col. 9, lns. 12-17. However, the invention in Bloom relates to an apparatus and method for hermetically sealing a fiber optic device. This is a distinctly different field of technology than that addressed in Jewell *et al* and the present application. Disclosure of positioning a fiber optic device 28 between a first substrate 204a and a second substrate 204b to form an enclosure 200 would in no way have made it obvious to the person skilled in the art to place an optical chip 28 on the underside of the chip 12 in the package disclosed in Jewell *et al*. The enclosure 200 of Bloom is meant to provide a hermetic seal, however, the package in Jewell *et al* is not concerned with hermetic sealing. To place an optical chip 28 on the underside of the chip 12 in the package disclosed in Jewell *et al* would be counter-intuitive as the chip 28 is intended to be attached to the macroscopic package 24. An optical chip 28 placed on the underside of the chip 12 in the package disclosed in Jewell *et al* would have no purpose or function.